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PTO/SB/21 (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/477,107
Filing Date	12/31/99
First Named Inventor	Christopher L. Hamlin
Group Art Unit	2131
Examiner Name	Dada, B. W.
Total Number of Pages in This Submission	
Attorney Docket Number	K35A0576

ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers *(for an Application)*
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) *(please identify below)*:

Post Card

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Howard H. Sheerin, Reg. 37,938
Signature	Howard H. Sheerin
Date	11/1/04

CERTIFICATE OF MAILING

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PTO/SB/17 (01-03)
Approved for use through 04/30/2003. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 340

Complete if Known	
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METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 23-1209

Deposit Account Name: WESTERN DIGITAL

The Commissioner is authorized to: *(check all that apply)*

☑ Charge fee(s) indicated below ☑ Credit any overpayments

☑ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		x 18.00 =	
Independent Claims		- 3** =		x 84.00 =	
Multiple Dependent				=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	340
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 340

SUBMITTED BY				(Complete *if applicable*)	
Name (Print/Type)	Howard H. Sheerin	*Registration No. (Attorney/Agent)*	37,938	*Telephone* 303-765-1689	
Signature	Howard H. Sheerin			*Date*	11/1/04

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, Washington, DC 20231.**

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In re Application of:
Christopher L. Hamlin
Serial No.: 09/477,107
Filed: 12/31/99
Title: INTEGRATED CIRCUIT COMPRISING ENCRYPTION CIRCUITRY SELECTIVELY ENABLED BY VERIFYING A DEVICE

Group Art Unit: 2131
Examiner: Dada, B. W.

BRIEF ON APPEAL

THE COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313

Sir,

The following appeal brief is submitted pursuant to the Notice of Appeal filed on 9/01/04, in the above-identified application.

REAL PARTY IN INTEREST

The real party in interest for the above-identified patent application is Western Digital Technologies, Inc. (see assignment REEL/FRAME: 011959/0188 identifying Western Digital Technologies, Inc. as assignee of the entire right, title and interest of the above-identified patent application).

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences related to the instant appeal.

STATUS OF CLAIMS

Claims 1-14 are the only claims pending and stand under final rejection. Claims 1-14 are the basis of this appeal.

STATUS OF AMENDMENTS

There are no outstanding amendments.

SUMMARY OF INVENTION

As illustrated in FIG. 1, the present invention may be regarded as an integrated circuit 100 for selectively encrypting plaintext data 102 received from a first device 104 to produce encrypted data 106 to send to a second device 108. The integrated circuit 100 comprises controllable encryption circuitry 110 comprising a data input 112, an enable input 114, and a data output 116. The integrated circuit 100 further comprises a plaintext input 118 for providing the plaintext data 102 to the data input 112, an encrypted text output 120 for providing the encrypted data 106 from the data output 116, and a first control input 122 for receiving a first device authentication signal 124 for authenticating the first device 104. A first verification circuit 130, responsive to the first device authentication signal 124, produces a first verification signal 132 for use in controlling the enable input 114 of the encryption circuitry 110 to enable the encryption circuitry 110 to provide the encrypted data 106 via the encrypted text output 120.

ISSUES

I. Whether claims 1, 3-8 and 10-14 are patentable under 35 U.S.C. §103(a) over Brown et al. (5,892,826) in view of Lewis (5,734,819).

GROUPING OF CLAIMS

Claims 1-14 stand rejected and are grouped together for the purpose of this appeal.

THE REFERENCES

The following references are relied upon by the examiner:

Brown et. al.	5,892,826	April 6, 1999
Lewis	5,734,819	Mar. 31, 1998
Le Rue	5,694,469	Dec. 2, 1997

THE REJECTIONS

Claims 1, 3-8 and 10-14 stand rejected under 35 USC §103(a) as unpatentable over Brown et al. in view of Lewis. The examiner asserts that Brown discloses encryption circuitry but concedes that Brown does not teach to authenticate a device that provides plaintext data before enabling the encryption circuitry. The examiner asserts that Brown could be modified in view of Lewis to arrive at the claimed invention since Lewis discloses to authenticate a device using a unique chip identifier.

ARGUMENT

I. THE ISSUE UNDER 35 U.S.C. §103(a) – BROWN IN VIEW OF LEWIS

A. The rejection should be reversed because modifying Brown in view of Lewis will not result in the claimed invention and therefore the examiner has failed to make a prima facie case of obviousness.

The rejection should be reversed because the examiner has failed to make a prima facie case of obviousness when the combination of references does not teach all of the claim limitations (MPEP 2143). In response to this argument, the examiner asserts the applicant is attacking the references individually rather than the combination. However, this interpretation of applicant's argument is incorrect. Modifying Brown in view of Lewis results in a combination that does not teach all of the claim limitations. It is only after the examiner interjects his own modifications in view of applicant's specification does the examiner arrive at all of the claim limitations.

The examiner concedes that Brown does not teach to authenticate a device before enabling an encryption circuit, but asserts that Lewis teaches this modification. However, Lewis discloses a system that authenticate a device before allowing software to run on the system (col. 5, lines 9-14). Therefore, modifying Brown in view of Lewis would result in a system that authenticates a device before allowing software to run on the system; it would not result in a system that authenticates a device before enabling encryption circuitry to operate as recited in the claims. Accordingly, the combination of references does not teach all of the claim limitations as required under MPEP 2143.

The suggestion to modify the prior art by authenticating a device before enabling encryption circuitry comes only from applicant's own disclosure which is not a proper basis to sustain a rejection under 35 USC §103.

CONCLUSION

Reversal of the rejections in this appeal is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 23-1209, and please credit any excess fees to such deposit account.

Respectfully submitted,

Date: 11/1/04 By: _____

Howard H. Sheerin
Reg. No. 37,938
Tel. No. (303) 765-1689

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on:

11/1/04 Howard H. Sheerin
(Date) (Print Name)

_____
(Signature)

APPENDIX

A complete listing of the claims on appeal:

1. An integrated circuit for selectively encrypting plaintext data received from a first device to produce encrypted data to send to a second device, the integrated circuit comprising:

controllable encryption circuitry comprising:

a data input;

an enable input;

a data output;

a plaintext input for providing the plaintext data to the data input;

an encrypted text output for providing the encrypted data from the data output;

a first control input for receiving a first device authentication signal for authenticating the first device; and

a first verification circuit, responsive to the first device authentication signal, for producing a first verification signal for use in controlling the enable input of the encryption circuitry to enable the encryption circuitry to provide the encrypted data via the encrypted text output.

2. The integrated circuit as recited in claim 1, further comprising:

a second control input for receiving a second device authentication signal authenticating the second device;

a second verification circuit responsive to the second device authentication signal for producing a second verification signal; and

a gating circuit responsive to the first and second verification signals for applying an enable signal to the enable input to cause the controllable encryption circuitry to provide the encrypted data via the encrypted text output.

3. The integrated circuit as recited in claim 1, wherein:

the first device authentication signal comprises a device identifier; and

the first verification circuit verifies the first device by comparing the device identifier to a corresponding expected device identifier.

4. The integrated circuit as recited in claim 3, wherein the expected device identifier is hardwired into the integrated circuit.

5. The integrated circuit as recited in claim 3, wherein:
the second device is a non-volatile memory; and
the expected device identifier is stored on the non-volatile memory.

6. The integrated circuit as recited in claim 1, wherein:
the first device authentication signal comprises a message authentication code generated over the plaintext data using a device key; and
the first verification circuit verifies the first device by verifying the message authentication code using an internal key.

7. The integrated circuit as recited in claim 1, wherein:
the first device is a signal processing circuit; and
the second device is a non-volatile memory.

8. A method of controlling encryption circuitry within an integrated circuit by selectively encrypting plaintext data received from a first device to produce encrypted data to send to a second device, the method comprising the steps of:
receiving the plaintext data from the first device;
receiving a first device authentication signal for authenticating the first device;
producing a first verification signal in response to the first device authentication signal; and
enabling the encryption circuitry in response to the first verification signal to provide the encrypted data to the second device.

9. The method of controlling encryption circuitry as recited in claim 8, further comprising the steps of:

receiving a second device authentication signal authenticating the second device;

producing a second verification signal in response to the second device authentication signal; and

enabling the encryption circuitry in response to the first and second verification signals to provide the encrypted data to the second device.

10. The method of controlling encryption circuitry as recited in claim 8, wherein:

the first device authentication signal comprises a device identifier; and

the step of producing a first verification signal in response to the first device authentication signal comprises the step of comparing the device identifier to a corresponding expected device identifier.

11. The method of controlling encryption circuitry as recited in claim 10, wherein the expected device identifier is hardwired into an integrated circuit.

12. The method of controlling encryption circuitry as recited in claim 10, wherein:

the second device is a non-volatile memory; and

the expected device identifier is stored on the non-volatile memory.

13. The method of controlling encryption circuitry as recited in claim 8, wherein:

the first device authentication signal comprises a message authentication code generated over the plaintext data using a device key; and

the step of producing a first verification signal in response to the first device authentication signal comprises the step of verifying the message authentication code using an internal key.

14. The method of controlling encryption circuitry as recited in claim 8, wherein:

the first device is a signal processing circuit; and

the second device is a non-volatile memory.